## ABSTRACT OF THE DISCLOSURE

A bit line contact structure and method for forming the same. After forming transistors on a substrate, Ti layer, TiN layer and W layer conformally cover the transistors and the substrate. The Ti/TiN/W stacked layer is defined to form an inner landing pad connecting to a source/drain region. A passivation layer is formed on the inner landing pad, the transistors and the substrate. An insulating layer with a flat surface is then formed on the passivation layer. A contact hole is formed in the insulating layer and the passivation layer to expose the inner landing pad. A M0 etching process is performed to form a recess of interconnecting landing pad patterns in the upper portion of the contact hole. An M0 deposition process is then performed.